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**Total Pages: 03** 

# BT-4/M-20

34104

# DIGITAL ELECTRONICS EE-202N

Time: Three Hours] [Maximum Marks: 75

**Note** AttemptFive questions in all, selecting atneeast question from each Unit.

### Unit I

- 1. (a) What are BCD code and Excess-3 code? What are the rules for BCD and Excess 3 code additions?Explain with suitable examples.
  - (b) Explain the rules of 1's complement 2'scomplements addition and subtraction with suitable examples.
- 2. (a) Explaindifferentypesof Logic gatesand theirtruth tables.8
  - (b) Describe De Morgan's theorems and simplify the given Boolean expression : **7**

Y(A, B, C, D
$$\neq \overline{(\overline{A} + C).(B + \overline{D})}$$

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## **Unit II**

3.	Minimizethe followingexpressionssing K-Map and	
	realize its using NOR gate only : 15	
	f(A, B, C, D) ≽m(0, 1, 3, 4, 5, 7, 10, 13, 14, 15	5)

**4.** Explain half subtractor and full subtractor and design full subtractor using half subtractor.

#### **Unit III**

- 5. (a) ExplainD/A and A/D convertewith Schematic diagrams.8
  - (b) DescribeSuccessiveApproximationMethod in detail. **7**
- 6. (a) Explain now a J-K flip-flop flow is converted in to D flip flop and T flip-flop.
  - (b) Praw a neat circuit diagram of clocked J-K flipflop using NAND gates. Give its truth table and explain race around condition. **7**

#### **Unit IV**

- 7. (a) Explain the characteristics f ECL family in detail.8
  - (b) Explain the operation of CMOS NOR gate.

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- 8. Write short notes onthereyof the following 5×3
  - (a) ROM
  - (b) PAL
  - (c) FPGA
  - (d) CPLDS.

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